METHOD OF READING A CAPACITIVE SENSOR AND RELATED INTEGRATED CIRCUIT

Field of the Invention

The present invention relates to the field of capacitive sensors, and more particularly to methods and integrated systems for reading a plurality of capacitors of a capacitive sensor including an array of capacitors.

Background of the Invention

Capacitive sensors are largely used as contact or pressure sensors. According to a particular embodiment, they may comprise an array of capacitors ordered in rows and columns connected through row and column lines (or plates), as schematically depicted in Fig. 1. These sensors produce a distribution map of the pressure even on a relatively large surface. The capacitance of each single capacitor of these sensors depends on the degree of deformation undergone by the dielectric layer of the capacitor, induced by a compressive force exerted thereon. By reading the values of the capacitances of all the capacitors of the array, an "array" of values ("frame") describing the spatial distribution of the pressure field on the sensing surface of the sensor is obtained.

The pressure field on the sensing surface may be easily displayed by a gray scale image, in which the luminance of each pixel is a function of the measured capacitance of a corresponding capacitor of the array.

Several problems have so far prevented realization of relatively low cost systems for reading such capacitive pressure sensors with good precision and with a great flexibility of use such to make them usable in particularly demanding applications. The precision of the sensing (reading) system of these sensors is negatively affected by the fact that the reading of the capacitance of a capacitor of the array is disturbed by the presence of the other capacitors and by parasitic capacitances between adjacent rows and columns. The capacitances affecting the reading of a single capacitor may add up to be 2 or 3 orders of magnitude greater than the capacitance of the selected capacitor being read to be detected. Moreover, a truly multipurpose system suitable to be used in many types of applications should work properly even if it is necessary to vary from time to time the number of addressable rows and columns of the array, depending on the particular application.

Summary of the Invention

It is an object of the present invention to provide a method and a system for reading a capacitive sensor that overcomes the above mentioned problems. The system of the invention can be realized in monolithic form and at a relatively low cost and may be used with sensors of different numbers of rows and columns.

More precisely the invention includes a method for reading a capacitive sensor formed by an array of capacitors ordered in rows and columns functionally connected through row lines, each one electrically constituting a first plate in common to all the capacitors of a row, and through column lines,

each one electrically constituting a second plate in common to all the capacitors of a column; the two sets of plates being orthogonal or quasi-orthogonal to each other. The method of the invention may be implemented by a circuit for biasing and reading capacitances that includes circuits for selecting a column line and a row line, and a charge amplifier producing an output voltage representing the capacitance of the selected capacitor intercepted by the selected column and row lines.

The method includes preliminarily resetting the output voltage of the charge amplifier, connecting to a reference voltage all the deselected row and column plates of the array and connecting an auxiliary capacitor and the selected capacitor to an inverting input of the amplifier and as feedback capacitor of the amplifier, respectively, or vice versa, and applying a step voltage on the capacitor that is connected to the inverting input of the amplifier and reading the output voltage at steady-state.

The reading method of the invention contemplates the scanning of all the capacitors of the array, to obtain as many values of capacitances. This "array" of values may be periodically updated at a certain "frame frequency", to display the way the distribution map of the pressure on the sensor area evolves in time.

The integrated reading system for a capacitive sensor of the invention comprises an input interface circuit connected to the capacitive sensor, forcing to a reference potential all deselected row plates and the column plates of the array and coupling to a biasing and reading circuit of the system the selected capacitor intercepted by the selected row and the selected column. The system also includes a biasing and reading circuit, producing an output voltage representative of the capacitance of the

selected capacitor coupled thereto; an analog-to-digital converter in cascade of the biasing and reading circuit converting the representative voltage in a corresponding bit vector; a microprocessor unit controlling the functioning of the system; and an output interface circuit functionally coupled to the microprocessor unit, outputting the read values of capacitance.

Brief Description of the Drawings

The different aspects and advantages of the invention will become even more evident through the following detailed description of several embodiments and by referring to the attached drawings, wherein:

Figure 1 is a schematic diagram depicting the array of capacitors of a capacitive sensor;

Figure 2 is a functional diagram of the integrated system of the invention according to a preferred embodiment;

Figure 3 is a detailed diagram of the input interface of the system of the invention;

Figure 4 is a schematic diagram showing a biasing and reading circuit according to a first embodiment of the invention;

Figure 5 is a schematic diagram showing a biasing and reading circuit according to another embodiment of the invention;

Figure 6 is a schematic diagram shows a preferred embodiment of the biasing and reading circuit suited to implement any of the two different embodiments of the method of the invention;

Figure 7 is a functional diagram of the input interface circuit;

Figure 8 is a schematic diagram showing an embodiment of the circuit for coupling the selected capacitor to be read to the biasing and reading circuit.

Detailed Description of the Preferred Embodiments

A preferred embodiment of the system of the invention, that may be readily integrated, is depicted in Fig. 2, in the form of block diagram. It includes an input interface block ANAIO, a biasing and reading block READOUT, an analog to digital conversion block ADC, a control block COMPUTING CORE and an output digital interface DIGITALI/O. In practice, the input interface ANAIO couples the selected capacitor C_{PIX} to be read to the biasing and reading circuit READOUT producing a voltage signal V_o representative of the capacitance of the read capacitor and grounds the plates of substantially all deselected capacitors of the sensor array. An analog-to-digital converter ADC converts the analog voltage V_0 in a corresponding multibit datum of bit vector.

The processing and control function are executed via an internal bus INTERNAL PERIPHERAL BUS by a control block COMPUTING CORE that comprises a microprocessor unit μP, ROM, RAM and BRIDGE. The control may also optionally and preferably involve a waveform generator WAVEFORM GENERATOR. This generator WAVEFORM GENERATOR that is controlled by the microprocessor unit, generates the signals for synchronizing the various functioning phases of the circuit READOUT and of the analog-to-digital conversion circuit ADC of the voltage V_o. The use of a dedicated generator WAVEFORM GENERATOR is particularly convenient, because it facilitates the programming of an optimized generation of such timing signals. A suitable waveform generator can be easily implemented by employing a ring register that is configured by a finite states machine controlled by the microprocessor unit, as will be readily recognized by a skilled technician.

The actual connections of input interface block are stage is depicted in a greater detail in Fig. 3. The interface ANAIO is connected to the capacitive

array sensor through a plurality of pins of the chip, for coupling the selected row and column plates (lines) of capacitors of the sensor to the circuit READOUT.

Two alternative embodiments of the system of the invention are exemplified in Figs. 4 and 5. Both employ a charge amplifier that represents the sensing element of the READOUT block. The charge amplifier is constituted by an operational amplifier with a non inverting input (+) connected to a ground potential and an inverting input (-) that is coupled to the capacitor to be read and to a feedback capacitor.

According to the embodiment depicted in Fig. 4, the selected capacitor C_{PIX} to be read is coupled to the input (-) of the operational amplifier, while the feedback capacitor C_R is a conventionally connected and is dischargeable by the shortcircuiting switch S1.

The method of reading the capacitance of C_{PIX} includes:

(a) resetting the voltage V_O by momentarily closing the switch S1;

(b) connecting the selected row and column plates to a reference potential;

(c) applying a step voltage V_I to the selected capacitor C_{PIX} connected to the input (-) of the amplifier, sensing at steady-state the voltage V_O.

In this way, the voltage V_O is subject to a variation ΔV_O proportional to the variation ΔV_I of the voltage V_I, according to the following formula:

$$\Delta V_O = \Delta V_I \cdot \frac{C_{PIX}}{C_R}$$

The charge injection into the feedback capacitor C_R, by the neighboring capacitors of the selected capacitor and by the parasitic capacitances C_{COL} and C_{ROW}, is effectively nullified because all deselected rows and columns are grounded.

According to an alternative embodiment,

depicted in Fig. 5, connection of the selected capacitor Cpix and of the feedback capacitor Cr may be inverted by connecting the selected capacitor C_{PIX} to be read as feedback capacitor and by connecting the auxiliary capacitor C_R to the input (-) of the amplifier. According to this alternative embodiment of the biasing and sensing circuit there will be a variation of the output voltage ΔV_O given by

$$\Delta V_O = \Delta V_I \cdot \frac{C_R}{C_{PIX}}$$

that is the output voltage presents a variation that, differently from the first embodiment, is inversely proportional to the selected capacitance C_{PIX}.

The two alternative configurations of Figs. 4 and 5 may be implemented with the same integrated circuit as the one depicted in Fig. 6, in which, by acting on the configuration switches controlled by a logic signal FEEDBACK, the selected capacitor to be read C_{PIX} may be coupled to the input and the auxiliary capacitor C_R connected as feedback capacitor to the charge amplifier or viceversa.

To make the input interface ANAIO suited to support array sensors of different number of rows and columns, it is realized, as depicted in Fig. 7, by a plurality of identical connection modules ANAIOCIRCUIT, each connected to a respective pin that are controlled by a dedicated selection logic ANAIOCONTROL. Each connection module ANAIOCIRCUIT, that may be realized as depicted in Fig. 8, connects a respective row or column of the sensor array to a reference potential or to the biasing and reading circuit READOUT, in function of selection signals ISIN, SELTHIS that are generated by a selection logic circuit controlled by the microprocessor unit.

A monolithically integrated system of the invention with such a modular input interface circuit,

may be used with capacitive sensors having any number of rows and columns of capacitors, provided that the sum of the number of rows and columns does not exceed the number of input channels (modules) of the input interface. In the case the modules of the input interface of the device are more numerous than the sum of rows and columns of the array of capacitors of the sensor to be used, the redundant connection circuits that are not used for coupling a respective row or column connect the respective pin of the device to a reference potential, as if they were connected to deselected rows or columns, without affecting the normal functioning of the integrated system.

Naturally, the method of the invention can be implemented by sequentially scanning the capacitors of the array for producing an array of values representing the map distribution of the quantity (pressure) detected by the capacitive sensor. Such a sequential scan may be repeated with a desired frequency ("frame frequency") for continuously refreshing the image of the distribution map of the pressure on the sensing area of the sensor.

Each frame of values so produced may be subjected by the microprocessor unit to noise filtering and to appropriate real-time correction processes such as the "gamma correction" and the "fixed pattern noise cancellation", before being output through a conventional digital output interface DIGITALI/O. To these purposes, the microprocessor unit will include a RAM of sufficient capacity for storing calculated capacitance values, besides a conventional ROM for storing information relating system's configuration and to the communication protocol employed.